

ABSTRACT OF THE DISCLOSURE

A memory circuit and method for reducing gate oxide stress is disclosed. The circuit includes a memory cell for storing data. The memory cell has a first 106 and a second 110 control terminal and a pass transistor 102. The pass transistor has a control gate coupled to the first control terminal. The memory circuit includes a drive circuit 900 having an output terminal 912 coupled to the second control terminal. The drive circuit is arranged to produce a control signal PL having a rise time and a fall time, wherein the fall time is greater than the rise time.

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